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(54) Method and device for analog programming of flash EEPROM memory cells with autoverify

(57) Device for analog programming comprising a current mirror circuit (19) connected to the drain terminals of a cell to be programmed (2) and of a MOS reference transistor (27); an operational amplifier (31) having inputs connected to the drain terminals (13) of the cell (2) and respectively of the MOS transistor (27) and output connected to the control terminal (30) of the MOS transistor. During programming, the control and drain terminals of the cell (2) are biased at corresponding programming voltages and the output voltage of the operational amplifier (31), which is correlated to the current threshold voltage level of the cell (2), is monitored and the programming is interrupted when this output voltage becomes at least equal to a reference voltage correlated to the threshold value desired for the cell.

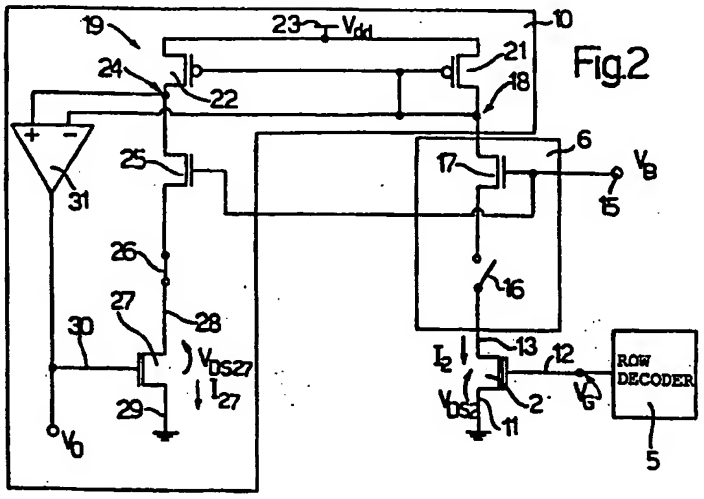

Fig.2

EP 0 905 712 A1

Description

[0001] The present invention relates to a method and a device for analog programming of flash EEPROM memory cells with autoverify.

[0002] As is known, and shown by way of example in Fig. 1, a flash memory array 1 comprises a plurality of flash cells 2 disposed on lines and columns, in which the gate terminals of the cells 2 disposed on one and the same line are connected to a respective word line 3, the drain terminals of the cells 2 disposed on one and the same column are connected to a respective bit line 4 and the source terminals are generally connected to ground. The word lines 3 are connected to a row decoder 5 and the bit lines 4 are connected to a column decoder 6 which receive respective address and control signals from a control unit 7 which permits the selection, from time to time, of a single word line 3 and a single bit line 4 and the biasing of the cell 2 connected to the word line and to the bit line selected at the operating voltages provided.

[0003] In particular, a cell 2 may be read by connecting the selected word line 3 to an external voltage V_G of preset value (such as 8-9 V) and forcing a biasing current I_f into the selected bit line 4. Keeping the selected cell in linear region, the following equation applies:

$$I_f = K^* (W/L)^*[(V_G - V_{th}) - V_{DS}/2]^*V_{DS} \qquad (1)$$

in which K is a constant associated with the production process, W/L is the dimensional width/length ratio of the cell, V_{th} is the threshold voltage of the cell (or the minimum voltage to be applied between the gate and source terminals of the cell so that it begins to conduct current) and V_{DS} is the drain/source drop of the cell. In (1) the term $K^*(W/L)^*V_{DS}=GM_f$ represents the transconductance (gain) of the cell and the term $(V_G - V_{th})$ represents the overdrive of the cell.

[0004] By suitably biasing the cell, the drop V_{DS} is constant and the term $V_{DS}/2$ is negligible with respect to the overdrive $(V_G - V_{th})$; consequently, in this state the current I_f flowing through the cell depends linearly on the threshold voltage V_{th}.

[0005] During writing (programming) of the cell, the latter is selected by biasing the selected word and bit lines at respective preset programming voltage values. Writing takes place thanks to the phenomenon of hot electron injection, whereby the high voltage supplied to the drain terminal of the cell to be written causes an increase in the velocity of the electrons and some of them achieve sufficient energy to overcome the barrier of the oxide. By forcing on the gate terminal a voltage which is higher than the drain terminal, the electric field which is created accelerates the electrons through the layer of oxide which separates the channel region from the floating gate region and permits the trapping of those electrons inside the floating gate region. The cell modifies its threshold voltage because of this trapping of the electrons.

[0006] By its nature, the phenomenon of hot electron injection is not controlled and not repeatable with accuracy; consequently, at the present time, during programming, the cell is read several times for reading the threshold voltage reached (verify phase).

[0007] This procedure is far from optimal, however, in view of the long periods of time required because of the need to interrupt programming, measure the threshold level reached and supply a new programming pulse. To overcome these problems for EEPROM memory cells, a system of programming and simultaneous verification of the programming has already been proposed (see US-A-5,422,842; US-A-5,495,442 and US-A-5,532,964 for example) which consists of measuring the current flowing through the cell during programming and comparing it with a reference current; as soon as the measured current becomes equal to or lower than the reference one, programming is interrupted.

[0008] The object of the invention is therefore to provide a method and a device which permit the verification of the threshold reached by flash-EEPROM cells during programming.

[0009] The present invention provides a method and a device for analog programming of flash EEPROM memory cells with autoverify, as defined in Claims 1 and 4 respectively.

[0010] For an understanding of the invention, preferred embodiments will now be described, purely by way of non-exhaustive example, with reference to the accompanying drawings in which:

- Fig. 1 shows a simplified circuit diagram of a flash memory of known type;
- Fig. 2 shows a simplified circuit diagram of the present programming and verify device;
- Fig. 3 shows a more detailed circuit diagram of the present device; and
- Fig. 4 shows the plot of significant electrical variables of the present device.

[0011] Fig. 2 shows the programming and verify device 10 as connected to a cell to be read 2 belonging to the memory array 1 shown in Fig. 1. For reasons of simplicity, of the array 1 Fig. 2 shows only the cell to be read 2 addressed via the row decoder 5 and the column decoder 6; the row decoder 5 has been omitted and only the essential elements of the column decoder 6 have been shown.

[0012] In particular, as shown in Fig. 2, the cell to be read 2 has source terminal 11 connected to ground, gate terminal 12 biased at the programming voltage V_G and drain terminal 13 connected to a node 18 via a selector switch 16 and a first biasing transistor 17 of NMOS type, both belonging to the column decoder 6 of

Fig. 1. The node 18 is connected to a current mirror device 19 formed by two PMOS transistors 21, 22; in detail, the PMOS transistor 21 is diode-connected (i.e. it has short-circuited drain and gate terminals) and has drain terminal connected to the node 18, source terminal connected to the supply line 23 set at V_{dd} and gate terminal connected to the gate terminal of the PMOS transistor 22; this latter has source terminal connected to the supply line 23 and drain terminal connected to a node 24.

[0013] Via a second biasing transistor 25 also of NMOS type and a dummy switch 26 kept closed at all times, the node 24 is connected to the drain terminal 28 of a reference transistor 27, of NMOS type, having source terminal 29 connected to ground and gate terminal 30 connected to the output of an operational amplifier 31; this latter has inverting input connected to the node 18 and non-inverting input connected to the node 24. The second biasing transistor 25 has gate terminal connected to the gate terminal of the first biasing transistor 17 and to a biasing node 15 to which a biasing voltage V_B is supplied. The biasing transistors 17 and 25 have the function of biasing the cell 2 and the reference transistor 27 at the desired voltage on the basis of the operating condition provided.

[0014] Fig. 2 also shows the output voltage V_o of the operational amplifier 31, also forming the output voltage of the programming and verify device 10; the voltage drop $V_{DS,2}$ and $V_{DS,27}$ between the drain and source terminals of the cell to be read 2 and, respectively, the reference transistor 27; as well as the currents I_2 and I_{27} flowing through the cells.

[0015] European patent application No. 97830172.9 entitled "High-precision analog reading circuit for memory arrays, in particular analog flash memory arrays" filed on 15.4.97 in the name of the same applicant, incorporated here for reference, describes a read device structurally similar to that of Fig. 2, in which a flash cell similar to the cell 2 is provided in place of reference transistor 27. For this device to which European application No. 97830172.9 relates, it has been shown, as briefly reported below, that the output voltage V_o of the operational amplifier 31 is linearly dependent on the threshold voltage $V_{th,2}$ of the cell 2. In fact, on the basis of (1), the current I_2 flowing through the cell to be read 2 and the current I_R flowing through the reference cell are expressed by:

$$I_2 = K^* (W/L)^*[(V_G - V_{th,2}) - V_{DS,2}/2]^*V_{DS,2} \quad (2)$$

$$I_R = K^* (W/L)^*[(V_o - V_{th,R}) - V_{DS,R}/2]^*V_{DS,R} \quad (3)$$

in which $V_{th,2}$ and $V_{th,R}$ are the threshold voltages of the cell to be read 2 and of the reference cell respectively, $V_{DS,R}$ is the source/drain drop of the reference cell and the other variables have the meaning already explained.

[0016] In the read condition, by assuming that the PMOS transistors 21 and 22 belonging to the current mirror device 19 and the biasing transistors 17 and 25 work at saturation, we have:

$$I_2 = I_R \quad (4)$$

[0017] Furthermore, in the equilibrium condition, the voltages at the inputs of the operational amplifier 31 (voltages at the nodes 18 and 24) are equal and, given that the biasing transistors 17, 25 receive, at the gate terminal, a same biasing voltage V_B (of 1.2-1.4 V for example), they have the same gate-to-source drop; it follows that if we admit equal voltage drops at the terminals of the selector switch 16 and the dummy switch 26, we have:

$$V_{DS,2} = V_{DS,R} \quad (5)$$

[0018] From (2) and (3), and taking account of (4) and (5), we obtain:

$$V_G - V_{th,2} = V_o - V_{th,R} \quad (6)$$

[0019] From (7) we also immediately obtain:

$$V_o = V_G - (V_{th,2} - V_{th,R}) \quad (7)$$

[0020] From (7) we see that the output voltage V_o of the amplifier 31 is linearly dependent on the threshold voltage $V_{th,2}$ of the cell to be read 2, so that the reading of this output voltage V_o supplies the threshold value $V_{th,2}$, knowing the threshold voltage of the reference cell R and the read voltage V_G applied to the gate terminal 12 of the cell to be read 2.

[0021] In the case of the device of Fig. 2, during reading, (7) is still valid, given that (1) also applies to the reference transistor 27 and assuming equal values for the parameters K, W and L.

[0022] At the start of programming, a high voltage V_B is supplied to the gate terminal of the biasing transistors 17, 25 so as to bring the drain terminal 13 of the cell to be programmed 2 to the programming drain voltage (7-8 V for example); a high voltage V_G (12 V for example) is also applied to the gate terminal 12 of the cell 2. In this condition, hot electrons are injected into the floating gate region of the cell 2 which thus gradually modifies its threshold voltage. In this phase, the currents I_2 and I_{27} are no longer equal but are nonetheless correlated and the output voltage V_o is still linearly dependent on the instantaneous threshold voltage of the cell 2. As the programming of the cell 2 continues and its threshold voltage increases, the current I_2 flowing in the cell 2 decreases, the voltage at the node 18 increases, the output voltage V_o and hence the voltage at the gate terminal of the reference transistor 27 decreases and its current I_{27} decreases; in particular, the reduction of the current I_{27} is substantially equal to the decrease of the current I_2 flowing in the cell 2, as can also be seen from Fig. 4 showing the plot of the currents I_2 and I_{27} for the

cell 2 and the transistor 27 versus the gate voltage V_G for two different threshold voltage values corresponding to two different moments of programming. In particular, the curves A and B refer to current I_2 of cells 2 having threshold voltages $V_{th'}$ and $V_{th''}$, where $V_{th'} < V_{th''}$ and the curves C and D refer to the plots of current I_{27} in the conditions of the curves A and B. In practice, during programming, the current characteristics of the cell 2 and of the reference transistor 27 move contemporaneously downwards because of the increase of the threshold voltage of the cell 2 and of the corresponding reduction of the gate voltage of the reference transistor 27.

[0023] In this way, by reading the output voltage V_o of the device 10, it is possible to monitor the programming phase instant by instant and interrupt it when the cell 2 has reached the desired threshold value.

[0024] Fig. 3 shows a more complete embodiment of the device 10, equipped with means for automatically interrupting the programming when the desired threshold voltage is reached, and with means of compensation of the loop formed by the components 31, 27, 26, 25 and 22.

[0025] In addition to the elements of Fig. 2, Fig. 3 shows a comparator 36, having a first input connected to the output of the operational amplifier 31 and a second input receiving a reference voltage V_{TAR} representing the target voltage, correlated to the threshold voltage desired for the cell 2; the output of the comparator 36 is connected to a selection input 37a of a switch 37 selectively connecting one of two nodes 37b, 37c to the biasing node 15. The node 37b is connected to a first voltage source 38 supplying the programming biasing voltage V_H and the node 37c is connected to a second voltage source 39 supplying the read biasing voltage V_L of lower value.

[0026] Fig. 3 further shows a compensation capacitor 40, a compensation transistor 41 and a current source 42. In detail, the compensation capacitor 40 is connected between the node 24 and a node 43; the current source 42 is arranged between the supply line 23 and the node 43 and the compensation transistor 41, of PMOS type, has its source terminal connected to the node 43, its gate terminal connected to the output of the operational amplifier 31 and its drain terminal connected to ground. These elements thus compensate for the loop 31, 27, 26, 25 which constitutes a two-stage amplifier, the first stage of which is formed by the operational amplifier 31 and the second stage uses the reference transistor 27 as amplifier element and in which the biasing transistor 25 operates as a cascode element which supplies a high impedance to the output of the loop (node 24).

[0027] Finally, Fig. 3 shows a capacitor 45, shown by broken lines and representing the parasitic capacitance of the bit line to which the cell to be read 2 is connected; the transistors (of NMOS type) which form the switches 16 and 26 and a reset transistor 44, of NMOS type, having the drain terminal connected to the intermediate node between the transistors 16 and 17, the source terminal connected to ground and the gate terminal receiving a control signal R.

[0028] In the device of Fig. 3, at the start of the programming phase, when the gate programming voltage V_G is supplied to the gate terminal 12 of the cell 2, the cell has low threshold voltage, the output V_o of the operational amplifier 31 is greater than the target voltage V_{TAR} (which, on the basis of (7), is equal to the programming gate voltage value V_G minus the desired threshold value and minus the threshold voltage value of the reference transistor 27) and the comparator 36 keeps the switch 37 in the position connecting the node 37b to the node 15. The node 15 is thus supplied by the high voltage V_H and the cell 2 begins to be programmed.

[0029] When, on increase of the threshold of the cell 2, the voltage V_o reaches the target value V_{TAR}, the comparator switches, bringing the switch into the position connecting the node 37c to the node 15. The node 15 is thus supplied at low voltage V_L and programming of the cell 2 is interrupted.

[0030] The above-mentioned system operates with high accuracy for medium-low values of the drain-to-source voltage V_{DS} in which the characteristic of the flash cell and of the MOS transistor change in the same way with respect to the drain-to-source voltage. For high values of this voltage, the existing structural differences (so-called "short channel" effect of the flash cell, on the basis of which the drain current of the cell increases much more quickly than that of the MOS transistor, which flattens out, as can also be seen from the graphs of Fig. 4) are such as to reduce the accuracy provided by this device. To solve this problem it is possible to use the simultaneous autoverify procedure solely in the first part of the programming phase in which high accuracy is not necessary. Subsequently, as the desired threshold value is approached, it is advisable to use the traditional programming system, sending programming pulses and then verifying, by means of a flash reference cell equal to the memory cell to be programmed, that the desired threshold has been reached, as described in the above-mentioned European patent application. In this case, with respect to the diagram of Fig. 3, a further comparator may be provided which is similar to the comparator 36 and receives a reference voltage correlated to a value which is lower than V_{TAR}; this comparator may control a further switch which may switch off the reference transistor 27 (by acting on the dummy transistor 26, for example, which would operate like a selection transistor for this purpose) and switch on a reference cell equal to the cell 2 downstream of the biasing transistor 25.

[0031] The advantages of the described method and device are as follows. Firstly, they permit an extremely speedy method of programming, including in the case of use solely in the first part of the programming, due to at least partial elimination of the dead times for interrupting programming, reading the threshold reached volt-

age and deciding as to whether to continue programming or not. Furthermore, the device is simple, occupies a reduced space in the memory and is reliable.

[0032] Finally it will be clear that numerous modifications and variants may be introduced to the method and the device described and illustrated herein, all of which come within the scope of the inventive concept as defined in the accompanying claims.

Claims

1. A method for analog programming of a flash EEPROM memory cell, characterized in that it comprises the steps of:

   - connecting a current source (19) with two outputs to a first terminal (13) of said cell (2) and to a first terminal (28) of a MOS transistor (27);
   - supplying a first voltage to a control terminal (12) of said cell, connecting said first terminal of said cell and said first terminal of said MOS transistor to a second voltage and connecting a second terminal (11) of said cell (2) and second terminal (29) of said MOS transistor to a reference potential, said first and second voltage being of amplitude such as to program said cell;
   - connecting said first terminals of said cell and of said MOS transistor to a first and a second input of a negative feedback element (31) and connecting an output of said negative feedback element to a control terminal (30) of said MOS transistor;
   - monitoring the output voltage of said negative feedback element (31) while said first terminal (13) of said cell (2) is connected to said second voltage and comparing said output voltage with a reference voltage; and
   - interrupting the supply of said second voltage to said first terminal of said cell when said output voltage becomes at least equal to said reference voltage.

2. A method according to Claim 1, characterized in that said output voltage is proportional to a current threshold voltage level of said cell (2) and in that said reference voltage is proportional to a desired threshold voltage level desired of said cell.

3. A method according to Claim 1 or 2, characterized in that said negative feedback element is an operational amplifier (31).

4. A device for analog programming of a flash EEPROM memory cell, connected to a memory cell (2) having a first (13) and a second (11) terminal and a control terminal (12), characterized in that it comprises:

   - a MOS transistor (27) having a first (28) and a second (29) terminal and a control terminal (30),
   - first and second current generating means (21, 22) generating a first and, respectively, a second current correlated to each other, said first current generating means (21) being connected to said first terminal (13) of said cell (2) and said second current generating means (22) being connected to said first terminal (28) of said MOS transistor (27);
   - negative feedback means (31) having a first and a second input connected to said first terminal (13) of said cell (2) and, respectively, said first terminal (28) of said MOS transistor (27) and an output connected to said control terminal (30) of said MOS transistor.

5. A device according to Claim 4, characterized in that said negative feedback means comprise an operational amplifier (31) having an inverting input connected to said first terminal (13) of said cell (2) and a non-inverting input connected to said first terminal (28) of said MOS transistor (27).

6. A device according to Claim 4 or 5, characterized in that said first and second current generating means (21, 22) form a current mirror circuit (19).

7. A device according to one of Claims 4-6, characterized in that it comprises a first (17) and a second (25) biasing transistor interposed between said first current generating means (21) and said first terminal (13) of said cell (2) and, respectively, between said second current generating means (22) and said first terminal (28) of said MOS transistor (27), said first and second biasing transistor having respective control terminals connected to each other (15) and receiving a common biasing signal.

8. A device according to Claim 7, characterized in that it comprises a comparator element (36) having a first and a second input and an output; said first input of said comparator element being connected to said output of said negative feedback element (31); said second input of said comparator element receiving a reference voltage and said output of said comparator element being connected to a control terminal (37a) of a two-position switch (37) connected to a first and a second biasing voltage and

to said control terminals of said first and second biasing transistor (17, 25); said switch, in a first commutation position, connecting said first input to said control terminals of said biasing transistors and, in a second commutation position, connecting said second input to said control terminals of said biasing transistors.

9. A device according to one of Claims 4-8, characterized in that said first terminal (13, 28) of said cell (2) and of said MOS transistor (27) is a drain terminal, said second terminal (11, 29) of said cell and of said MOS transistor is a source terminal and said control terminal (12, 30) of said cell and of said MOS transistor is a gate terminal.

10. A device according to one of Claims 4-9, characterized in that it comprises a compensation circuit (40-42) interposed between said first terminal (28) of said MOS transistor (27) and said output (30) of said negative feedback means (31).

11. A device according to Claim 10, characterized in that said compensation circuit (40-42) comprises a compensation capacitor (40) and a compensation transistor (41), said compensation capacitor (40) having a first terminal connected to said first terminal (28) of said MOS transistor (27) and a second terminal connected to a first terminal (43) of said compensation transistor (41), said compensation transistor having a control terminal connected to said output (30) of said negative feedback means (31).

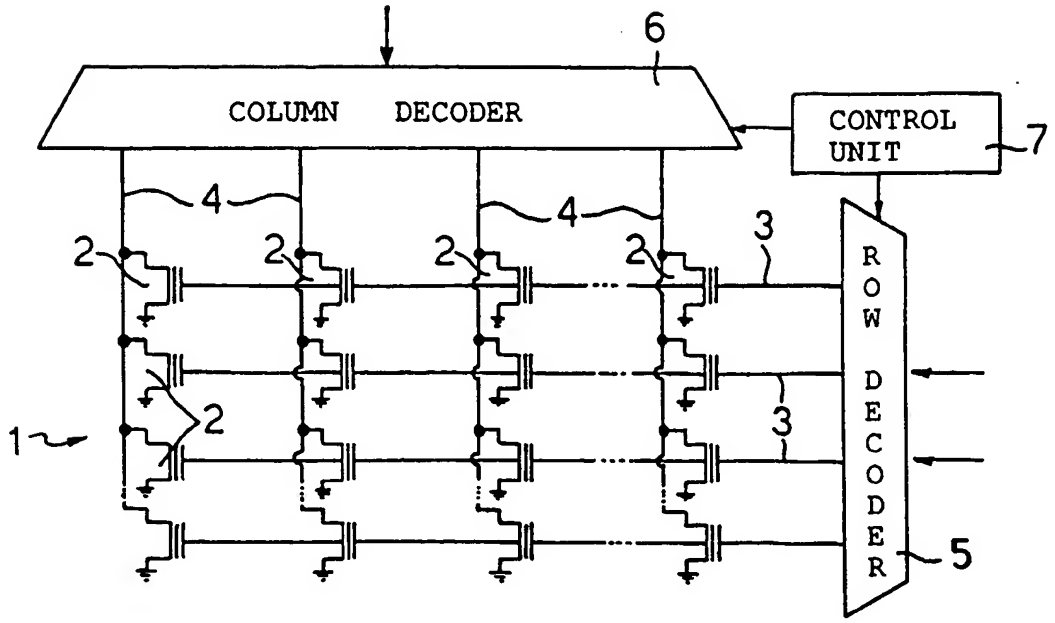

Fig.1

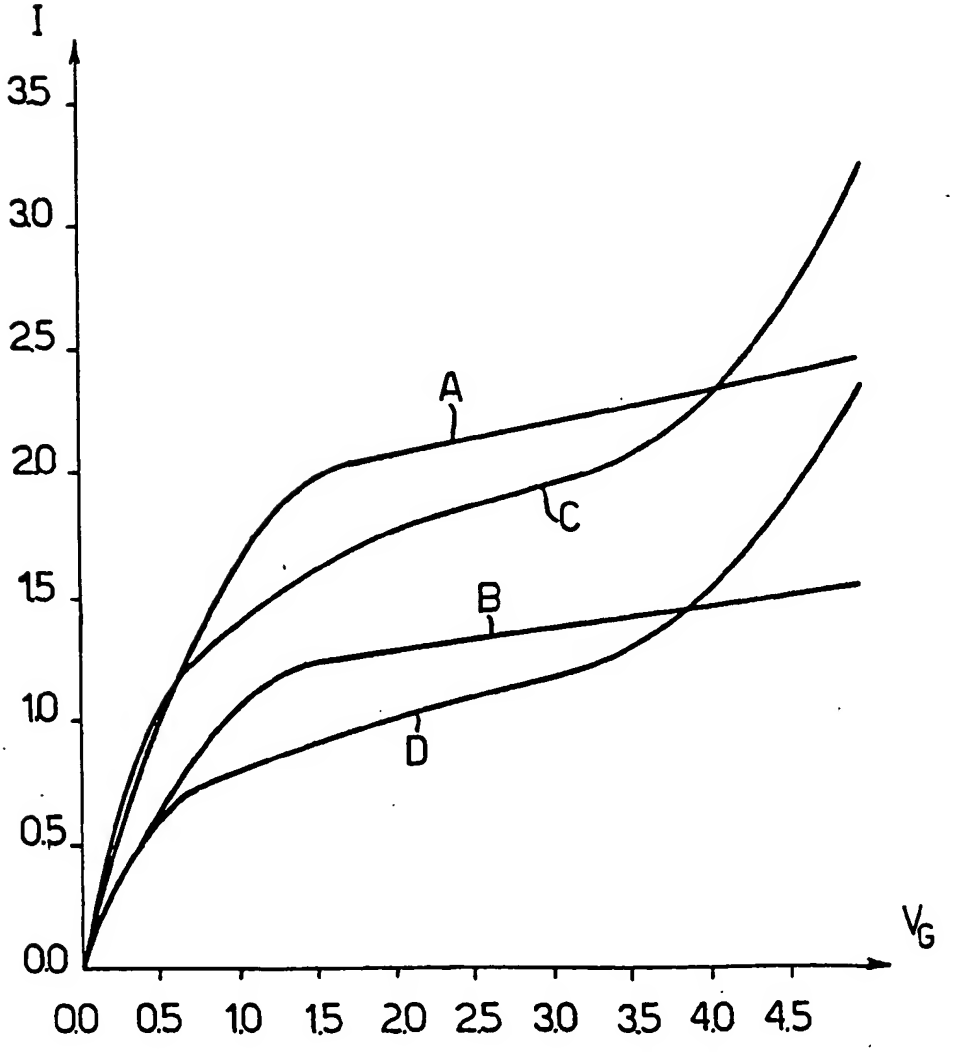

Fig.4

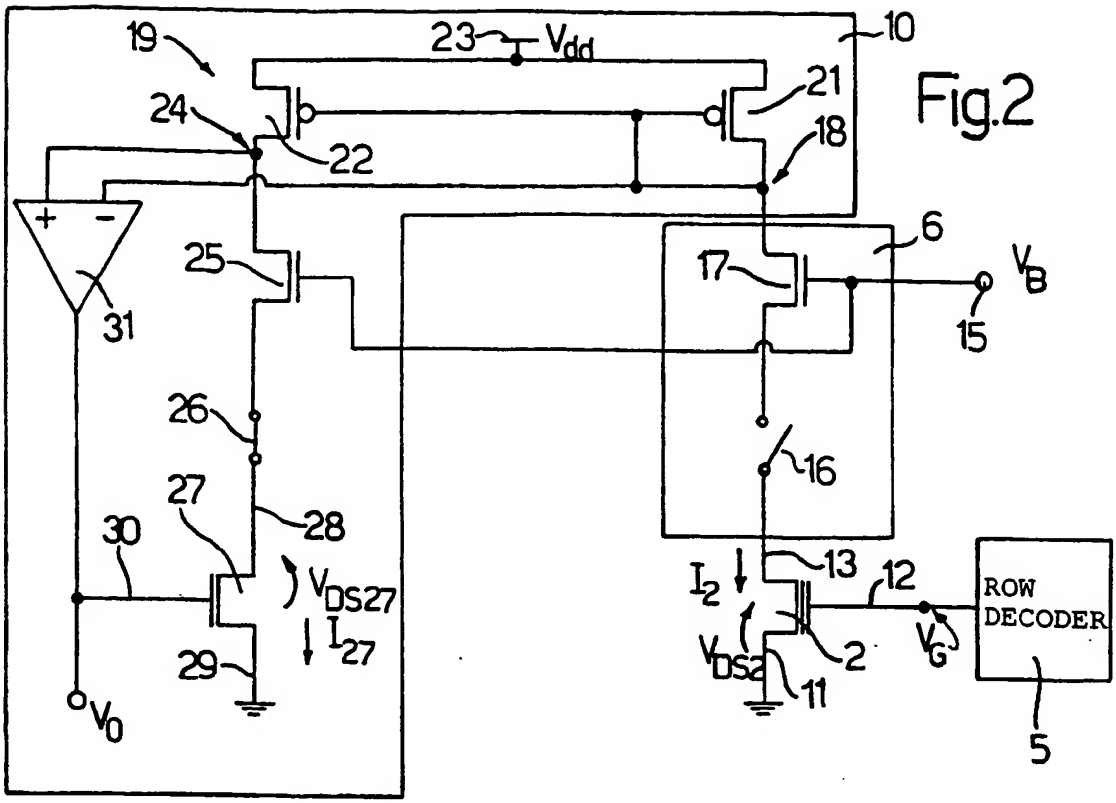

Fig.2

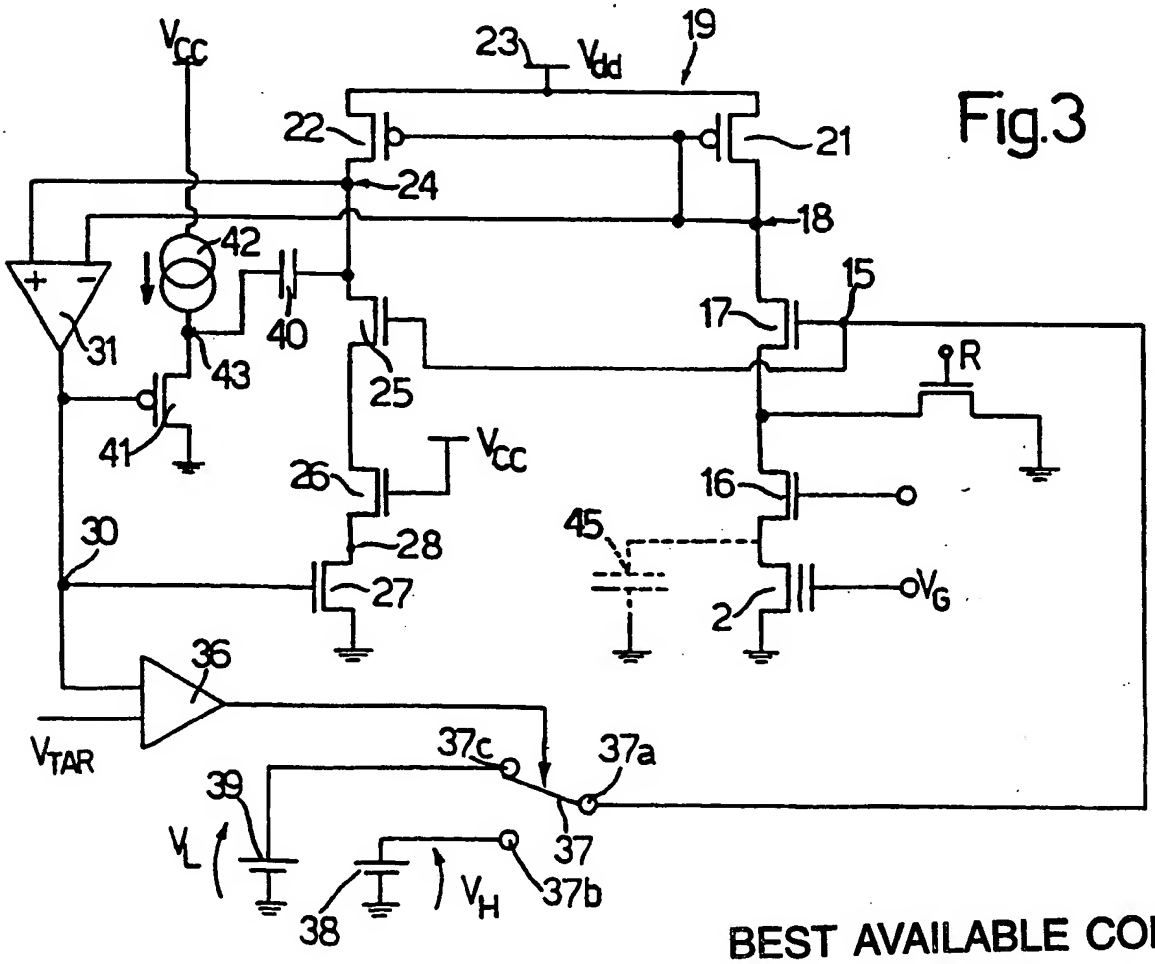

Fig.3

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EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0477

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 606 522 A (CHAI YONG-YOONG) * column 3, line 16 - column 7, line 20; figures 1,5 *	1,2,4,9	G11C27/00
A	US 5 555 521 A (HAMADA MINORU ET AL) * column 12, line 57 - column 15, line 52; figure 10 *	1,3-5,7, 8	
A	FUJITA O ET AL: "CHARACTERISTICS OF FLOATING GATE DEVICE AS ANALOGUE MEMORY FOR NEURAL NETWORKS" ELECTRONICS LETTERS, vol. 27, no. 11, 23 May 1991, pages 924-926, XP000213694 * the whole document *	1,3-5	
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 420 (P-1267), 24 October 1991 & JP 03 171494 A (MATSUSHITA ELECTRIC IND CO LTD), 24 July 1991, * abstract; figure 3 *	1,4	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 March 1998	Cummings, A

CATEGORY OF CITED DOCUMENTS

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